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Claims

[c1] 1.A method for selective electroplating of a semiconductor input/output (I/O) pad, the method comprising:
forming a titanium-tungsten (TiW) layer over a passivation layer on a semiconductor substrate, said TiW layer further extending into an opening formed in said passivation layer for exposing the I/O pad, such that said TiW layer covers sidewalls of said opening and a top surface of the I/O pad;
forming a seed layer over said TiW layer;
selectively removing portions of said seed layer such that remaining seed layer material corresponds to a desired location of interconnect metallurgy for the I/O pad; and
electroplating at least one metal layer over said remaining seed layer material, using said TiW layer as a conductive electroplating medium.

[c2] 2.The method of claim 1, wherein said seed layer further comprises a Cu/CrCu layer.

[c3] 3.The method of claim 1, wherein said at least one metal layer further comprises a nickel layer followed by a gold layer.

[c4] 4.The method of claim 1, further comprising removing portions of said TiW layer not covered by said at least one metal layer following electroplating thereof.

[c5] 5.The method of claim 1, wherein the I/O pad further comprises an aluminum pad.

[c6] 6.The method of claim 1, wherein said seed layer is selectively removed by photoresist patterning.

[c7] 7.The method of claim 1, wherein said passivation layer further comprises a photosensitive polyimide (PSPI) layer.

[c8] 8.A semiconductor input/output (I/O) pad structure, comprising:
a titanium-tungsten (TiW) layer formed into an opening formed in a passivation layer on a semiconductor substrate, said opening created for exposing an I/O pad, such that said TiW layer further covers sidewalls of said opening and a top surface of said I/O pad;
a seed layer formed over a portion of said TiW layer and corresponding to a desired location of interconnect metallurgy for said I/O pad; and
at least one metal layer electroplated over said seed layer, wherein said TiW layer serves as a conductive electroplating medium.

[c9] 9.The I/O pad structure of claim 8, wherein said seed

layer further comprises a Cu/CrCu layer.

[c10] 10.The I/O pad structure of claim 8, wherein said at least one metal layer further comprises a nickel layer followed by a gold layer.

[c11] 11.The I/O pad structure of claim 8, wherein said I/O pad further comprises an aluminum pad.

[c12] 12.The I/O pad structure of claim 8, wherein said at least one metal layer partially encapsulates a sidewall of said seed layer.

[c13] 13.The method of claim 12, wherein said at least one metal layer covers a remaining portion of said TiW layer not covered by said seed layer.

[c14] 14.The method of claim 8, wherein said passivation layer further comprises a photosensitive polyimide (PSPI) layer.